# Electric field effects in ultrathin $\beta$-ZrNBr nano-crystals

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Layered materials with a non-zero band gap have emerged in the past few years because of their potential to supersede graphene in nano-electronics. Zirconium nitrogen halides (ZrNX, X = Cl,Br) are indirect gap semiconductors with a layered crystal structure. Here, we report the realization of electric field effects in exfoliated nano-crystals of $\beta$-ZrNBr using degenerately doped silicon as a back-gate. The as-produced devices demonstrate n-type transport with field effect carrier mobility of 5.8 $cm^2\ V^{-1}\ s^{-1}$. The conduction is dominated by variable range hopping for the range of temperature from 295 K to 32 K. Our results present a promising candidate for future thin-film electronics application. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4816504]

The isolation of 2-dimensional crystals of layered semiconductors with a non-zero band gap[1] has been the focus of intense research efforts due to the various kinds of practical applications these materials may have in digital electronics,[2–5] optoelectronics,[6] sensors,[7] lithium batteries,[8] hydrogen storage,[9] as well as the possible new physics that may evolve from the fundamental studies on the exotic nature of their electronic states.[10–12] Of particular interest are the related studies of layered metal chalcogenides,[13,14] transition metal oxides (e.g., $MoO_3$ and $La_2CuO_4$),[15,16] hexagonal boron nitride (h-BN),[17] and the topological insulators $Bi_2Se_3$, $Bi_2Te_3$, and $Sb_2Se_3$.[18–21] The common feature of these materials is that they have a three-dimensional crystal structure consisting of stacked layers that are interacted by weak van der Waals forces between adjacent layers.

In compounds like graphite and layered metal dichalcogenides, the electronic structures of the layered crystals are usually modified by intercalation.[22,23] The $\beta$-polymorph of transition metal nitrogen halides, MNX (M = Zr, Hf; X = Cl, Br), has a similar layered crystal structure which can be exploited, to add charge carriers by means of intercalation, thereby modifying their electronic structures to induce superconductivity.[24,25] Alternatively, the weak interlayer van der Waals forces enable their exfoliation into thin crystalline nano-sheets with atomically flat surfaces, thus allowing for the tuning of the number of charge carriers with an applied electric field. Recently, an electric double-layer transistor was implemented by ionic-liquid gating to induce superconductivity in the host compound of $\beta$-ZrNCl, with a superconducting transition temperature of 15.2 K.[26] Herein, we report the implementation of a field effect transistor based on exfoliated ultrathin nano-crystals of $\beta$-ZrNBr, using degenerately doped silicon as a back-gate. The as-produced field effect transistors exhibit n-type transport. The conduction is dominated by variable range hopping for the range of temperature from 295 K to 32 K. The field effect mobility is 5.8 $cm^2\ V^{-1}\ s^{-1}$ at room temperature and decreases at low temperature suggesting that the mobility is limited by charge impurity scattering. Our results present a promising material for future thin-film electronics application beyond silicon era.

The crystal structure of ZrNBr consists of stacked six-layer slabs of Br-Zr-N-N-Zr-Br where the atoms within each slab are bonded by strong covalent and ionic interactions. These slabs are subsequently stacked and retained together by weak Br-Br van der Waals forces (Figure 1(a) inset). The layered ternary ZrNBr exists in two polymorphs: $\alpha$- and $\beta$-forms with the FeOCl- and SmSI- structure type, respectively. Here, we study the $\beta$-ZrNBr form (SmSI-type), where double sheets of Zr-N-N-Zr are sandwiched between close-packed layers of bromide atoms. $\beta$-ZrNBr is characterized as a semiconductor with an observed band gap of 3.2 eV.[27]

In experiment, $\beta$-ZrNBr bulk crystals were obtained from a two-step synthesis. First step involved reacting zirconium foil (Aldrich, 99.98%) with two molar equivalents of ammonium bromide (Aldrich, 99.999%) in an evacuated quartz tube (1 cm diameter, ~15 cm length) at 600 °C for four days.[28] To prevent the reaction tube from exploding, the total loading mass was limited to 100 mg, and the furnace temperature was slowly increased from 150 °C. In the second step, the resulting green product was reground with $NH_4Br$ in a 5:1 (ZrNBr to $NH_4Br$) ratio and recrystallized by chemical transport for 2 weeks under a temperature gradient of 750–850 °C. The resulting transparent green plate-like crystals of the title compound were formed at the hot end of the gradient and were found to be highly crystalline with diameters of about 0.5 mm.

Several representative crystals were ground and characterized via X-ray powder diffraction, using a PANalytical X'Pert PRO diffractometer with $\theta$-$\theta$ geometry and a Cu K$\alpha$ source (Figure 1(a)). The polycrystalline sample was indexed, using X'Pert HighScore Plus program, to a hexagonal unit cell with parameters $a = 3.6410(4)$ and $c = 29.275(2)$. This agrees with the lattice parameters for

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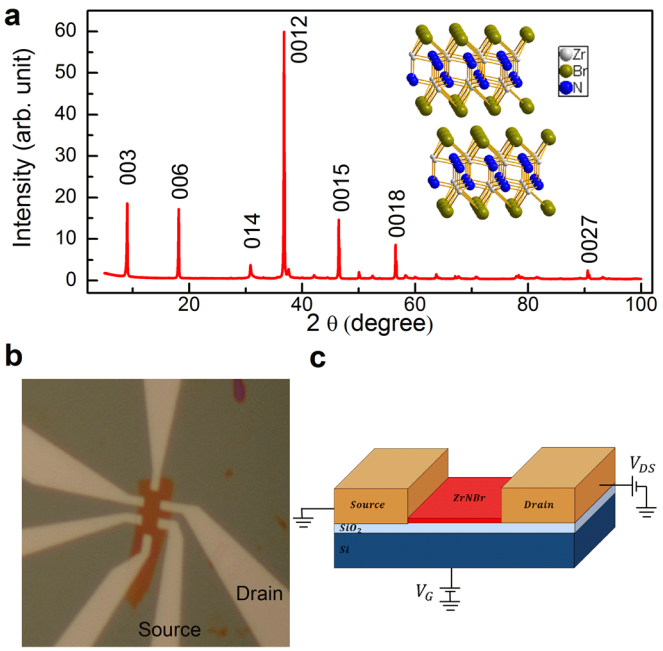


FIG. 1. (a) X-ray powder diffraction data for bulk $\beta$-ZrNBr sample. (Inset) A schematic diagram of the layered crystal structure of $\beta$-ZrNBr. (b) Optical micrograph of the device under study. The electron transport data presented in this paper are collected using the two electrodes marked as "Source" and "Drain." (c) A schematic diagram of the back-gate configuration of the device.

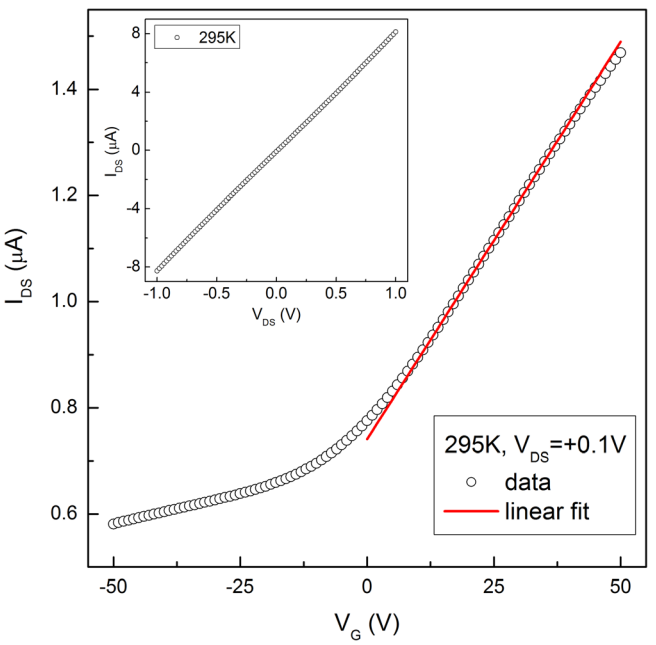


FIG. 2. (Open dot) Drain source current $I_{DS}$ as a function of back-gate voltage $V_G$, for fixed drain source voltage $V_{DS} = 0.1$ V at T = 295 K. (Solid line) Linear fit of the data from $V_G = +17$ V to $V_G = +32$ V. (Inset) $I_{DS}$ is plotted as a function of $V_{DS}$ for $V_G = 0$ V, at T = 295 K.

$\beta$-ZrNBr reported in the literature.[29] The enhanced diffraction intensities of the 00$l$ peaks show that the plate crystals, as expected, exhibited preferred orientation.

The $\beta$-ZrNBr bulk crystals were then mechanically exfoliated into thin nano-crystals using the Scotch tape method, on a silicon wafer covered with thermally grown 200 nm silicon dioxide. The nano-crystals were identified under an optical microscope. Electron-beam lithography was performed to define the metal electrodes (45 nm Pd on top of 5 nm Cr) electrically contacting the ZrNBr nano-crystal. An optical micrograph of the device is presented in Figure 1(b). Atomic Force Microscopy (AFM) revealed the thickness of the nano-crystal to be ~21 nm, which corresponds to approximately 22 layers. Although we designed a Hall-bar geometry device, the high sheet resistance at low temperatures restricted us to two terminal measurements. The two selected terminals are labeled as "Drain" and "Source" in the optical micrograph [Figure 1(b)]. The electrode width of 1 $\mu$m results in a metal-semiconductor contact area of ~1 $\mu m^2$. The gap between the drain-source is 1 $\mu$m and the conduction channel width is ~1.5 $\mu$m between the selected electrodes. We used the degenerately n-doped silicon as a back gate to tune the carrier density in the conduction channel. A schematic diagram of our device is illustrated in Figure 1(c). Electrical characterizations, from 295 K to 80 K, were performed using a Lakeshore cryogenic probe-station. Electrical experiments below 80 K were performed in a vacuum insert immersed in liquid helium.

The drain-source current $I_{DS}$ as a function of the drain-source voltage $V_{DS}$ is linear (Figure 2 inset) at room temperature, which demonstrates the ohmic contact between the metal electrodes and the semiconductor $\beta$-ZrNBr. In Figure 2, $I_{DS}$ is plotted as a function of the back gate voltage $V_G$, at fixed $V_{DS} = +0.1$ V. Our device manifests n-type transport. The $I_{DS}$ increase linearly with positive $V_G$. Calculating the slope of the linear fit of the data from $V_G = +17$ V to $V_G = +32$ V, we estimate the field effect charge carrier mobility $\mu$ to be 5.8 $cm^2\ V^{-1}\ s^{-1}$ using the formula

$$\mu = \left[\frac{\Delta I_{DS}}{\Delta V_G}\right] \times \frac{1}{V_{DS}} \times \left[\frac{L}{WC}\right],$$

where L = 1 $\mu$m is the length and W = 1.5 $\mu$m is the width of the conduction channel, $C = \frac{\varepsilon_0 \varepsilon_r}{d}$ is the capacitance per unit area of our back-gate configuration, $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m is the free space permittivity, $\varepsilon_r = 3.9$ is the relative permittivity of silicon dioxide, d = 200 nm is the dielectric thickness. For a negative gate voltage, the device behavior differs from a typical n-type field effect transistor where the channel is depleted of charge carriers and switches to an "off-state."[4,5] In contrast, here we observe that the current does not drop significantly, even though it continues to decrease, almost linearly, with negative gate voltage. The device cannot be turned off in spite of the fact that the channel is a semiconductor with a band gap of 3.2 eV. The residue current offset for negative gate voltage could be attributed to the presence of parallel conduction channels, as discussed in details later.

Fitting the data within $V_G = \pm 5$ V, the carrier mobility $\mu$ around zero gate voltage is evaluated to be 3.9 $cm^2\ V^{-1}\ s^{-1}$. Using Drude formula $\sigma = ne\mu$, we can estimate the inherent carrier concentration at zero gate voltage to be $\sim 8 \times 10^{12}$ $cm^{-2}$, where $\sigma$ is the conductivity and e is the charge of an electron. We attribute the inherent carriers to the presence of impurity donor levels close to the conduction band edge. The gate voltage induced carrier concentration $n' = \frac{\varepsilon_0 \varepsilon_r V_G}{de}$ at the largest applied gate voltage $V_G = 50$ V is calculated to be $\sim 5 \times 10^{12}$ $cm^{-2}$ which is comparable to the inherent carrier concentration at $V_G = 0$ V. This is consistent with the

observed effect of gate voltage on the drain-source current where we see a ~90% increase when we go from $V_G = 0$ V to $V_G = +50$ V. However, the current is reduced by only ~25% as we go from $V_G = 0$ V to $V_G = -50$ V. This asymmetry in $I_{DS}$-$V_G$ indicates a carrier mobility change which may result from a different screening behavior for negative and positive gate voltage. At positive gate voltage side, the n-type carrier concentration is higher, which leads to a better screening of charge impurity scattering and thus a larger carrier mobility (i.e., a resultant larger slope in $I_{DS}$-$V_G$ curves). On top of that, a fraction of the gate-voltage induced charges can be trapped as immobile charges at the interface between the sample and the dielectrics ($SiO_2$). These trapped surface charges do not contribute to electrical conduction and thus result in an effective lower field-effect-mobility (nominally obtained from the $I_{DS}$-$V_G$ data). Thus, the asymmetry in $I_{DS}$-$V_G$ curves may also be partly originated from a change of the density of such trapped surface states as a function of energy, e.g., the density of trapped states can be higher in the energy range for negative $V_G$ side while lower for positive $V_G$ side. Overall, the difference in both the screening strength and the density of trapped states can explain the observed asymmetric $I_{DS}$-$V_G$ curves with respect to the polarity of the applied gate voltage.

In addition, a complete off-state is not obtained at the largest applied negative $V_G$ (Fig. 2), which can be attributed to the screening effect due to relatively high carrier density and the parallel conduction in layered structures. With the thin-nanocrystal of ZrNBr as the conduction channel, the electric field induced by the bottom gate is screened rapidly yielding a small screening length $\lambda_s$, considering the relatively high inherent carrier density estimated as $8 \times 10^{12}\,cm^{-2}$ at $V_G = 0$. In accordance with the Thomas-Fermi approximation, the electrostatic potential $\varphi$ induced by the applied gate voltage drops exponentially with increasing distance z from the interface between the sample surface and the gate dielectrics, i.e., $\varphi(z) = \varphi(0)e^{-z/\lambda_s}$. For the ZrNBr nano-crystal with a thickness of 21 nm (~22 layers) and a relatively high carrier density, parallel conduction from different layers has to be considered, and thus a complete off-state could not be achieved within the applied $V_G$ range. Similar behaviors have been previously reported in multilayer graphene.[1,30–32]

In a semiconductor, the number of thermally excited carriers drops exponentially with decreasing temperature. This would affect the channel conduction and the screening of the electric field introduced by the gate voltage. Therefore, in order to understand the device physics better, we investigated the temperature dependence of the device performance from 295 K to 4.2 K. Figure 3(a) presents $I_{DS}$ as a function of $V_{DS} = \pm 1$ V, at zero gate voltage from 295 K to 80 K. The $I_{DS}$-$V_{DS}$ curve is linear at $T \geq 150$ K. At low temperatures below $T = 150$ K, as the thermal excitation is suppressed, a contact barrier is perceived and the $I_{DS}$-$V_{DS}$ curve becomes non-linear at 80 K (this is more noticeable in Figure 3(c)). In Figure 3(b), $I_{DS}$ is plotted as a function of $V_G$ from −50 V to +50 V at temperatures ranging from 295 K to 80 K. First we notice that the residue current offset at the negative $V_G$ side drops rapidly with lower temperature. This behavior deviates from the temperature dependence of other n-channel field effect transistors, such as $SnS_2$, where the number of carriers induced by the gate voltage is significantly higher than the inherent carriers at zero gate voltage.[4] In case of $SnS_2$, the residue current in the depleted state remains insignificant compared to the accumulated state at all temperatures. In the current study of $\beta$-ZrNBr, at low temperatures below $T = 120$ K, the device can be switched to a carrier depleted "off state" by applying negative gate voltage, while in contrast a complete "off state" is not achievable at $T \geq 150$ K. This can be explained as follows. At low temperatures as the number of mobile charge carriers is reduced, the screening length-which is inversely proportional to the square root of the carrier density[33]-increases and hence the carrier transport of the 21 nm thick $\beta$-ZrNBr crystal (conduction channel) can now be adequately controlled by gate-voltage-induced electric field. Also, the magnitude of conductance enhancement at positive $V_G$ (charge accumulation region) is smaller with decreasing temperature which can be explained by carrier mobility reduction.

As the temperature goes down from 80 K to 4.2 K, the conductance continues to decrease monotonically and the effect of the contact barrier becomes more prominent in electron transport. In Figure 3(c), we plot $I_{DS}$ as a function of $V_{DS}$ for temperatures from 80 K to 4.2 K. In this temperature range, in order to overcome the contact barrier, $I_{DS}$-$V_{DS}$ curves were measured within a larger $V_{DS}$ range: from −5 V to +5 V. Figure 3(d) presents $I_{DS}$ as a function of $V_G$ from −100 V to +100 V, for fixed $V_{DS} = +2$ V at different temperatures from 80 K down to 4.2 K. The saturation current, at $V_G \sim 100$ V, decreases with decreasing temperature as expected for reduced carrier concentration at low temperatures. However, the slopes of the linear portion of the $I_{DS}$-$V_G$ curves, which represent the maximum field effect mobility, do not change significantly in this temperature range from 80 K to 4.2 K.

From Figures 3(b) and 3(d), we extract the channel conductance as a function of temperature at $V_G = +20$ V and plot it in a logarithmic scale as a function of $T^{-1/3}$ (Figure 4(a)). The data at $V_G = +20$ V are chosen so that the Fermi level is near the conduction band edge while the conductance is still high enough to be measured accurately. In the temperature range from 295 K to 32 K, the data can be fitted well with the variable range hopping picture for charge transport in two dimensions[34]

$$G(T) = G(0)e^{\left(\frac{T_0}{T}\right)^{\frac{1}{3}}},$$

where G(0) is a constant conductance and $T_0$ is a constant temperature reflecting the correlation energy scale. This suggests that the electronic states in the system, at or near the Fermi level, may be localized and electrons hop from one state to another when gaining energy from a phonon or external applied electric field. From of the slope of the fit (Figure 4(a)), we estimate $T_0 \approx 5.8 \times 10^4$ K. Using $\sigma = e^2\left(\frac{dn}{dE}\right)D$ where the diffusion constant is given by Einstein relation as $D = \frac{\mu k_B T}{e}$ and the experimentally obtained carrier mobility $\mu = 5.8\ cm^2\ V^{-1}\ s^{-1}$ at $T = 295$ K, we obtain a density of states $\left(\frac{dn}{dE}\right) \approx 2.2 \times 10^{18}/eV\ m^2$. With that, we then estimate a localization length $\xi_{VRH} \approx 1$ nm from the equation[35] $\xi_{VRH} = \sqrt{\frac{13.8}{k_B\left(\frac{dn}{dE}\right)T_0}}$. Below $T = 32$ K, the data start to deviate

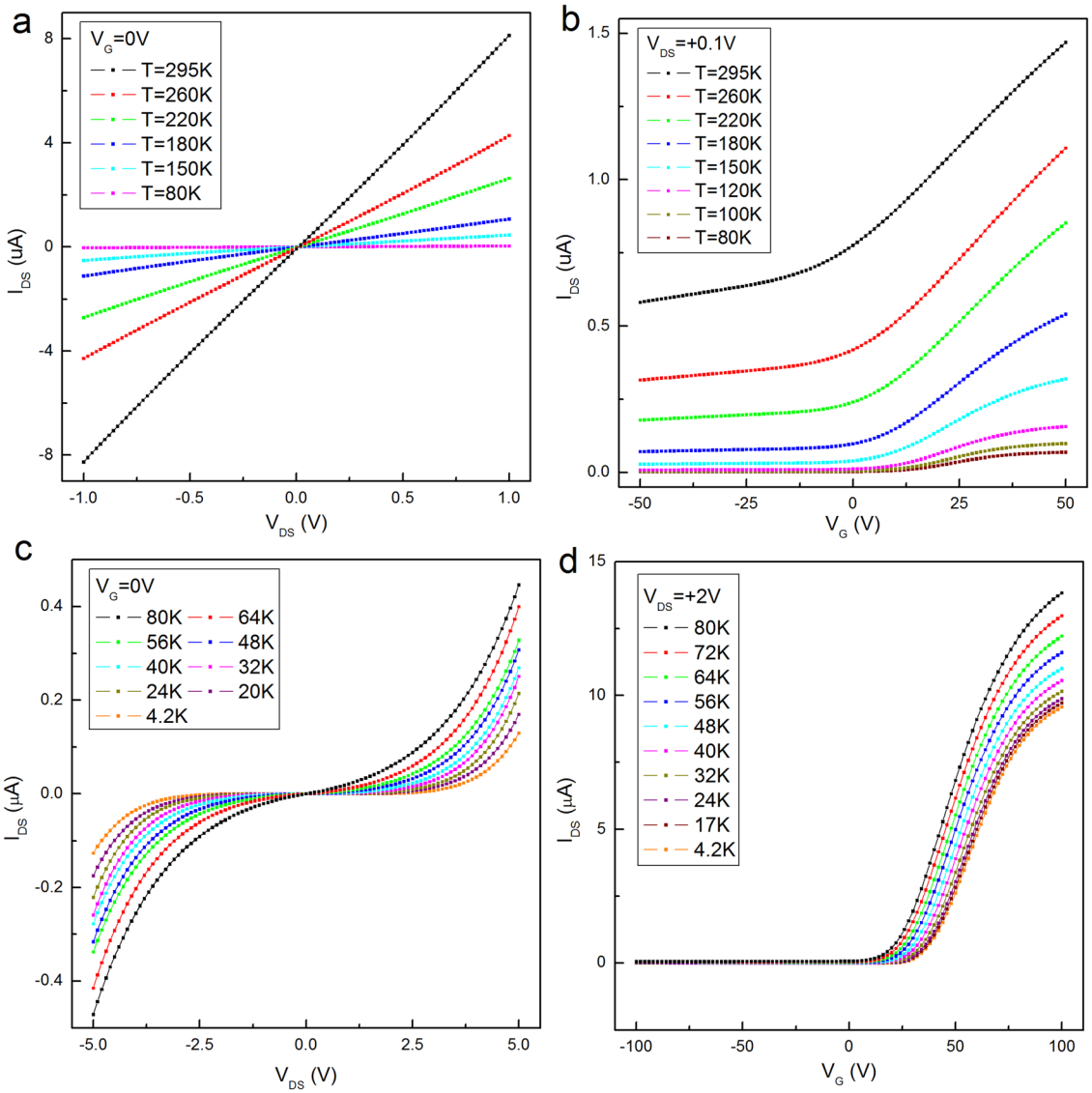


FIG. 3. (a) $I_{DS}$ as a function of $V_{DS}$ for zero back gate voltage $V_G$, at 295 K, 260 K, 220 K, 180 K, 150 K, and 80 K. (b) $I_{DS}$ as a function of $V_G$ for fixed $V_{DS} = +0.1$ V at 295 K, 260 K, 220 K, 180 K, 150 K, 120 K, 100 K, and 80 K. (c) $I_{DS}$ as a function of $V_{DS}$ for $V_G = 0$ V at 80 K, 64 K, 56 K, 48 K, 40 K, 32 K, 24 K, 20 K, and 4.2 K. (d) $I_{DS}$ is plotted versus $V_G$ for $V_{DS} = +2$ V at 80 K, 72 K, 64 K, 56 K, 48 K, 40 K, 32 K, 24 K, 17 K, 4.2 K.

from variable range hopping model and tend to develop a plateau, which could be explained by an enlarged size of localized electron puddles at low temperatures and thus a nearly temperature independent conduction. This behavior was also noticed recently in nano-structured anti-dot graphene samples.[35]

In Figure 4(b), the maximum field effect mobility is plotted as a function of temperature. The carrier mobility drops quickly as the temperature is lowered from 260 to 90 K (at a temperature range from 80 to 4.2 K, as shown by the data from a different measurement, the mobility continues to decrease at a slower rate). This suggests that the mobility is not limited by phonon scattering at room temperature. Otherwise, if phonon was the dominant scattering source, one would have observed an enhancement in carrier mobility with decreasing temperature, since electron-phonon scattering should be diminished at low temperatures. Instead, the decreasing mobility with decreasing temperature can be attributed to charge impurity scattering arising from random disorders (e.g., contaminations) near the conduction channel. More specifically, the reduced carrier density at low temperatures gives rise to a weakened screening of charge impurities, and consequently an enhanced impurity scattering causes lower carrier mobility with decreasing temperature. Therefore, the observed temperature dependence of the mobility suggests that impurity scattering, instead of intrinsic phonon scattering, is most likely the limiting factor for room temperature carrier mobility of FET devices under study.

In summary, field effect transistors based on exfoliated thin nano-crystals of ZrNBr (in the order of 10 nm) were implemented. The as-produced devices exhibited n-type transport with a relatively high field effect mobility of 5.8 $cm^2\ V^{-1}\ s^{-1}$. From low-temperature transport studies, we show that the mobility is constrained by impurity scattering rather than phonon scattering, which promises further mobility improvement by reducing charge impurities from contaminations introduced during the device fabrication. The carrier transport is found to be dominated by variable range hopping over a wide span of temperature from 295 to 32 K. Our results shed light on the nature of electron transport in a

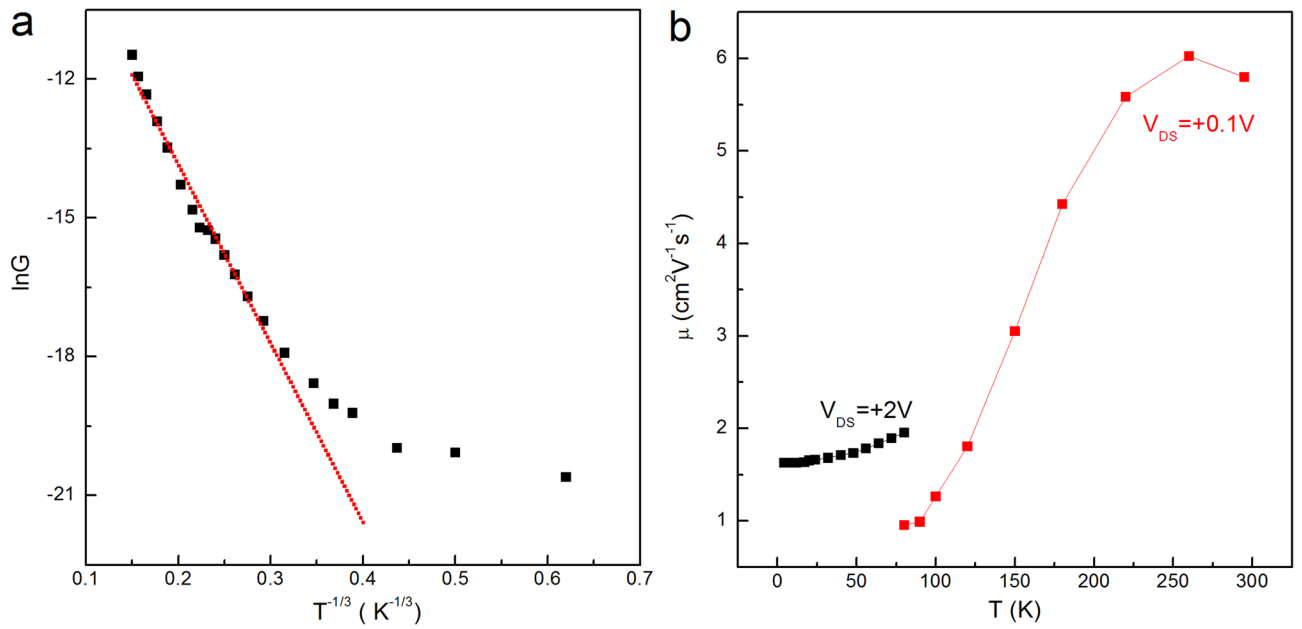


FIG. 4. (a) (Solid square) Drain-source conductance G plotted in a logarithmic scale as a function of $T^{-1/3}$. (Solid line) Linear fit of the data from 295 K to 32 K. The data are collected from different thermal cycles: one from 295 K to 80 K measured with a probe station, and another from 80 K to 4.2 K measured with a vacuum insert immersed in liquid helium. (b) Carrier mobility $\mu$ as a function of temperature T. The mobility is calculated at a fixed $V_{DS} = +0.1$ V for temperature range 295 K to 80 K and $V_{DS} = +2$ V for 80 K to 4.2 K. The jump of mobility data at T = 80 K is due to the different measurements from different thermal cycles with different experimental setup, as specified above.

host layered compound rarely studied up-to-date, which may be important for future nano-electronic applications beyond the era of silicon.

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